

**Due to errors in the learning outcome format of this syllabus, it has been removed and replaced with the original syllabus style.**

**The examination for 2007 will be set to this syllabus below. A revised format of this syllabus in learning outcome terms, which will fully reflect this syllabus, will be available as soon as possible. We apologise for any inconvenience caused but since the previous unit was only posted on the website in July 2007 we do not anticipate this change effecting candidates adversely.**

## **9107-231 COMPUTER SYSTEMS ENGINEERING**

### **AIMS**

To provide the student with the necessary knowledge and skills to design processor based computer systems.

To appreciate the effect of a processor's architecture on the performance of a system.

### **PREREQUISITES**

Candidates will be expected to be familiar with the relevant Certificate examination topics.

### **OUTCOMES**

A student should be able to:

1. undertake digital processor based design with the appropriate interfaces.
2. select suitable logic chips, architectures, languages and tools.
3. understand the effect the components of a system have on its overall performance

### **SYLLABUS**

#### **The Processor**

Load and store architecture, the use of a stack for arithmetic expressions, subroutine and interrupt handling

Zero, single and multiple address architectures, addressing modes including, but not limited to, immediate, relative, direct and indirect , pointer based addressing

Instruction formats: zero, single and multiple address instructions

Reduced Instruction Set Computer (RISC) versus Complex Instruction Set Computer (CISC)

## **Computer Arithmetic**

Floating point numbers and arithmetic: IEEE floating-point format, underflow, overflow, rounding, and truncation errors

Two's complement numbers, arithmetic and circuits: Adders (ripple, carry look ahead, carry save), subtractors, multipliers, dividers

## **Combinational and Sequential Circuits**

Analysis and design of, for example, counters, multiplexers, comparators, decoders, priority encoders, shift registers

Analysis and design of sequential logic using finite state machines.

## **Timing and Control**

Hardwired and microprogrammed control, status bits and their use in program control

Instruction cycle phases and timing diagrams

Dealing with interrupts and exceptions

## **High Performance Techniques**

Pipeline principles, problems and solutions, including data hazards and stalling, branch hazards and exceptions.

Pipelining for RISC and CISC architectures

Superscalar systems and dynamic pipelining

Parallel functional units, memory interleaving

Cache memories

Instruction level parallelism

Multiprocessor systems and associated problems: including consideration of speed versus number of processors issues, inter-processor communication issues

## **Memory Organisation**

Characteristics and use of different memory types

Single and multi-level cache memory – including reference to direct-mapped, set associative and fully associative placement

Static RAM, DRAM, ROM, optical memory, disc, tape

Timing cycle for RAM and ROM

Memory hierarchy and memory management

Virtual memory and addressing

### **Input-Output Interfacing**

Interface considerations: synchronous and asynchronous communication, handshaking, serial and parallel interfaces

Program controlled input/output, interrupt controlled input/output, including hardware for handling interrupts

Hardware and timing for Direct Memory Access (DMA)

Input-Output Processors

Designing an I/O system

### **Design Options**

Fixed function off-the shelf devices, logic families for example CMOS.

Clock speed issues

Programmable devices: characteristics and use of PLAs, PALs, PROMs, Field Programmable Gate-Arrays (FPGAs), standard cells.

Complex devices: microprocessors, memories, peripheral interfaces. Application Specific Integrated Circuits (ASICs).

### **Design Methodology**

Need for hierarchical design methodology: behavioural, structural and physical levels.

Design synthesis

Design capture tools: hardware description languages (for example Verilog, VHDL), schematic capture.

Testing strategies

### **ASSESSMENT**

Assessment will comprise of the following elements:

- a three-hour written examination designed to test the theoretical content specified in each unit outcome

## 9107-231 Reading List

### *Core Texts*

<b>Computer Organization and Design: The Hardware/Software Interface</b> 1558606041	David A. Patterson, John L. Hennessy	Morgan Kaufmann	Pbk	2004	£39.89
<b>Computer System Architecture (International Edition)</b> 0131757385	M. Morris Mano	Prentice Hall	3rd Ed. Pbk	1993	£46.99
<b>Logic and Computer Design Fundamentals Xilinx Student Edition 4.2 Package</b> (Intern'l Edition) 0131247891	M. Morris Mano, Charles R. Kime	Prentice Hall	3rd Ed	2003	£43.99
<b>Principles of Digital Design</b> 0132423979	Daniel D. Gajski	Pearson Education	Pbk	1996	£46.99